

FIG. 4

Isolation

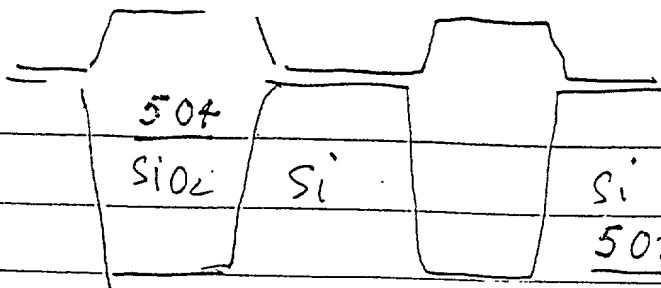


FIG. 5

VT and well implants

Channel stop

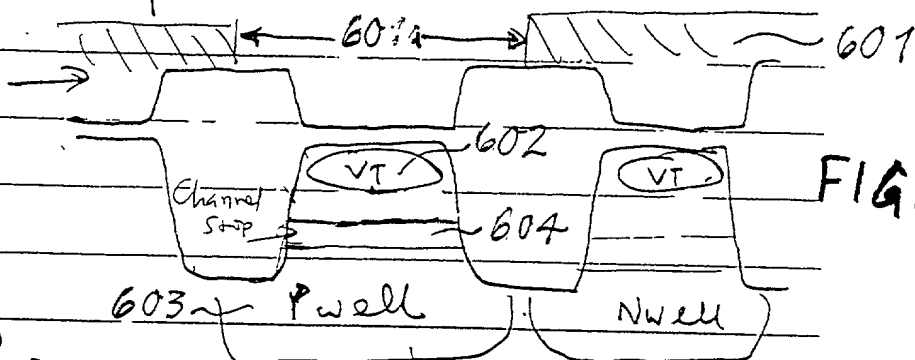


FIG. 6

Gate definition

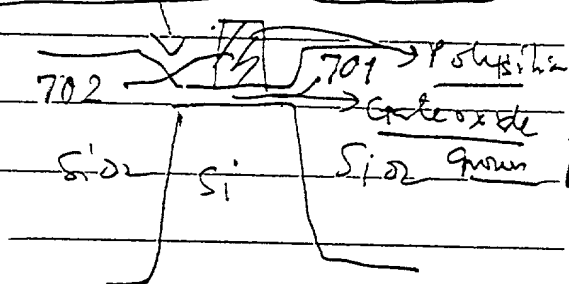


FIG. 7

NMOS & PMOS CDD & Pocket/
Implant Halo

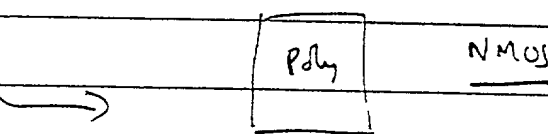
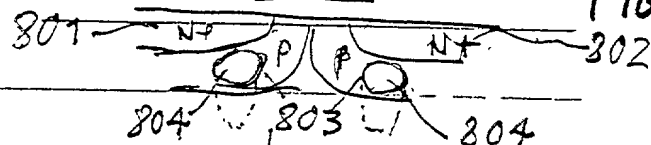


FIG. 8

Spacers + SD imp



Silicide formation

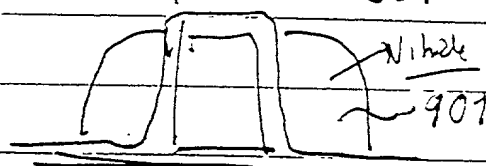


FIG. 9

PMD + Contact formation

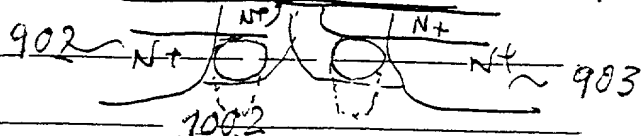


FIG. 10

Metal deposition
pattern

